AF/CW

Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: WATTS et al.

Application Serial No.: 10/729,544

Filing Date: December 5, 2003

For: STACKED INTEGRATED CIRCUIT PACKAGES AND METHODS OF MAKING THE PACKAGES

Confirmation No.: 1914

Group Art Unit: 2836

Examiner: Leonardo Andujar

Response Transmittal to Notification of Non-Compliant Appeal Brief (37 CFR 41.37) mailed 10/23/2006

Attorney Docket No.: P17173

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CERTIFICATE OF MAILING UNDER 37 CFR 1.8

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Dated: November 20, 2006 By: Edith Martin

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Sir:

Enclosed are:

1. ☑ Corrected Appeal Brief filed in response to Notification of Non-Complaint Appeal Brief mailed October 23, 2006
2. ☑ Appendix A – Claims
3. ☑ Appendix B - Evidence
4. ☑ Appendix C – Related Proceedings
5. ☑ Additional Enclosures: Acknowledgement Postcard

The Commissioner is hereby authorized to charge and credit Deposit Account No. 50-1852 as described below. A duplicate copy of this sheet is enclosed.

- ☑ Credit any overpayment.
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Respectfully submitted,

November 20, 2006
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Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit: 2826

Examiner: Leonardo Andujar

Appellants: WATTS et al.

Application Serial No.: 10/729,544

Filing Date: December 5, 2003

For: STACKED INTEGRATED CIRCUIT PACKAGES AND METHODS OF MAKING THE PACKAGES

CORRECTED APPEAL BRIEF (Filed in response to Notification of Non-Compliant Appeal Brief)

Attorney Docket No.: P17173

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CERTIFICATE OF MAILING UNDER 37 CFR 1.8

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Dated: November 20, 2006 By: Edith Martin

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Appellants hereby appeal to the Board of Patent Appeals and Interferences from the decision of the Examiner in the Final Office Action mailed June 16, 2006 (the "Final Office Action"), rejecting claims 15, 17-19, 21, 22, 34, 36, 37 and 39-43.

REAL PARTY IN INTEREST

The present application is assigned to INTEL CORPORATION, 2200 Mission College Blvd., Santa Clara, California 95052, U.S.A.

RELATED APPEALS AND INTERFERENCES

No other appeals or interferences are known to Appellants, Appellants' legal representative, or assignee, which will directly affect, be directly affected by, or have a bearing on the Board's decision in the pending appeal.

STATUS OF CLAIMS

Claims 15, 17-19, 21, 22, 34, 36, 37 and 39-43 are pending in this application. All pending claims stand rejected and are now being appealed.

Claims 1-14, 16, 20, 23-33, 35 and 38 have previously been canceled.

STATUS OF AMENDMENTS

No amendments are pending or were filed after the Final Office Action.

SUMMARY OF CLAIMED SUBJECT MATTER

The present application is concerned with a design for a stacked IC (integrated circuit) package which allows for manufacturing efficiencies and a reduced height of the resulting package. (Specification, page 10, lines 12-20.) In an example embodiment, a stacked IC package 100 (FIG. 4) is formed as a stack of identical package components 10. (Specification, page 9, lines 1-2.) Each package component 10 includes a substrate 12 on which an IC 106 is mounted (on the top surface 14 of the substrate 12). (Specification, page 9, lines 7-8.)

A coverlay 38 is laminated to the top surface 14 of each substrate 12. (Specification, page 4, lines 1-2.) There is a large central opening 40 (FIG. 1) formed in each coverlay 38.

(Specification, page 4, lines 7-8.) The central openings 40 (identified by reference numeral in FIG. 1 in a sample package component 10) each accommodate a respective IC 106 (shown in FIG. 4) mounted on the top surface 14 of the substrate 12. (Specification, page 4, lines 9-10.) Connections are made between ICs 106 by means of via metal 46 which traverses vertically through the coverlay 38. (Specification, page 9, lines 10-13.)

Each package component 10 also has a ground plane 28 (FIG. 1) formed on the lower surface 16 of its respective substrate 12. (Specification, page 3, lines 10-16.) The ground plane 28 is covered by a solder mask layer 34. (Specification, page 3, lines 21-22.)

* * * * * * *

Appellants will now, as required by the Notification of Non-Compliant Appeal Brief, map the independent claims, element to element, to the disclosure of this application.

Claim 15

"An article of manufacture": Stacked IC package 100 (FIG. 4); specification--page 9, lines 1-2.

"at least two integrated circuit (IC) packages in stacked relation to each other": Package components 10 (FIG. 4); specification --page 9, lines 1-2.

"each of the IC packages including"

"a substrate": Substrate 12 (FIG. 1, FIG. 4); specification--page 9, lines 7-8.

"an IC mounted on a first surface of the substrate": IC 106 (FIG. 4), top surface 14 of substrate 12 (FIG. 4, FIG. 1); specification--page 9, lines 7-8.

"a ground plane formed on an opposite surface of the substrate from the first surface on which the IC is mounted": Ground plane 28 (FIG. 1, also seen in FIG. 4 but not called out by reference numeral), lower surface 16 (FIG. 1, also seen in FIG. 4 but not called out by reference numeral); specification--page 3, lines 10-16.

"a coverlay formed of an organic material and laminated on the first surface of the substrate and having at least one opening formed by photolithography": Coverlay 38 (FIG. 1, FIG. 4), top surface 14 (FIG. 1), substrate 12 (FIG. 1), opening 40 (FIG. 1); specification, page 4, lines 1-9.

"at least one conductive connection formed through one of the coverlays and connecting one of the ICs to another of the ICs": metal 46 (FIG.1, FIG. 4), coverlays 38 (FIG. 1, FIG. 4), ICs 106 (FIG. 4); specification, page 9, lines 10-13; page 4, lines 9-14.

"each IC is positioned in an opening of a respective one of the coverlays": ICs 106 (FIG. 4), openings 40 (FIG. 1, also seen in FIG. 4 but not called out by reference numeral), coverlays 38 (FIG. 1, FIG. 4); specification, page 4, lines 9-10.

"the opening formed by photolithography": Opening 40 (FIG. 1, also seen in FIG. 4 but not called out by reference numeral); specification, page 4, lines 8-9.

"all of said each IC being in said opening of said respective one of the coverlays": ICs 106 (FIG. 4), opening 40 (FIG. 1, also seen in FIG. 4 but not called out by reference numeral), coverlays 38 (FIG. 1, FIG. 4).

Claim 19

"An apparatus": Electronic apparatus 120 (FIG. 5); specification, page 9, lines 24-25.

"stacked integrated circuit (IC) package": Stacked IC package 100 (FIG. 4, FIG. 5); specification--page 9, lines 1-2.

"a first substrate": Substrate 12 (FIG. 1, FIG. 4); specification--page 9, lines 7-8.

"a first IC mounted on a first surface of the first substrate": IC 106 (FIG. 4), top surface 14 of substrate 12 (FIG. 4, FIG. 1); specification--page 9, lines 7-8.

"a first ground plane formed on an opposite surface of the first substrate from the first surface on which the first IC is mounted": Ground plane 28 (FIG. 1, also seen in FIG. 4 but not called out by reference numeral), lower surface 16 (FIG. 1, also seen in FIG. 4 but not called out by reference numeral); specification--page 3, lines 10-16.

"a first coverlay formed of an organic material and laminated on the first surface of the first substrate and having at least one opening formed by photolithography": Coverlay 38 (FIG. 1, FIG. 4), top surface 14 (FIG. 1), substrate 12 (FIG. 1), opening 40 (FIG. 1); specification, page 4, lines 1-9.

" a second substrate positioned in stacked fashion on the first coverlay: Substrate 12 (FIG. 1, FIG. 4), coverlay 38 (FIG. 1, FIG. 4); specification--page 9, lines 7-8.

"a second IC mounted on a first surface of the second substrate": IC 106 (FIG. 4), top surface 14 of substrate 12 (FIG. 4, FIG. 1); specification--page 9, lines 7-8.

"a second ground plane formed on an opposite surface of the second substrate from the first surface on which the second IC is mounted": Ground plane 28 (FIG. 1, also seen in FIG. 4 but not called out by reference numeral), lower surface 16 (FIG. 1, also seen in FIG. 4 but not called out by reference numeral); specification--page 3, lines 10-16.

"a second coverlay laminated on the first surface of the second substrate and having at least one opening formed by photolithography": Coverlay 38 (FIG. 1, FIG. 4), top surface 14 (FIG. 1), substrate 12 (FIG. 1), opening 40 (FIG. 1); specification, page 4, lines 1-9.

"at least one conductive connection connecting the first IC to the second IC and passing through at least one opening in the coverlay": metal 46 (FIG.1, FIG. 4), coverlays 38 (FIG. 1, FIG. 4), ICs 106 (FIG. 4); specification, page 9, lines 10-13; page 4, lines 9-14.

"a communication device coupled to at least on of the first IC and the second IC": communication device 122 (FIG. 5), ICs 106 (FIG. 4); specification, page9, lines 25-27.

"the first IC is positioned in an opening formed by photolithography in the first coverlay": IC 106 (FIG. 4), opening 40 (FIG. 1, also seen in FIG. 4 but not called out by reference numeral), coverlay 38 (FIG. 1, FIG. 4); specification, page 4, lines 9-10.

"all of the first IC being in said opening formed by photolithography in the first coverlay": IC 106 (FIG. 4), opening 40 (FIG. 1, also seen in FIG. 4 but not called out by reference numeral), coverlay 38 (FIG. 1, FIG. 4).

"the second IC is positioned in an opening formed by photolithography in the second coverlay": IC 106 (FIG. 4), opening 40 (FIG. 1, also seen in FIG. 4 but not called out by reference numeral), coverlay 38 (FIG. 1, FIG. 4); specification, page 4, lines 9-10.

"all of the second IC being in said opening formed by photolithography in the second coverlay": IC 106 (FIG. 4), opening 40 (FIG. 1, also seen in FIG. 4 but not called out by reference numeral), coverlay 38 (FIG. 1, FIG. 4).

Claim 34

"An article of manufacture": Stacked IC package 100 (FIG. 4); specification--page 9, lines 1-2.

"at least two integrated circuit (IC) packages in stacked relation to each other": Package components 10 (FIG. 4); specification --page 9, lines 1-2.

"each of the IC packages including"

"a substrate": Substrate 12 (FIG. 1, FIG. 4); specification--page 9, lines 7-8.

"an IC mounted on a first surface of the substrate": IC 106 (FIG. 4), top surface 14 of substrate 12 (FIG. 4, FIG. 1); specification--page 9, lines 7-8.

"a ground plane formed on an opposite surface of the substrate from the first surface on which the IC is mounted": Ground plane 28 (FIG. 1, also seen in FIG. 4 but not called out by reference numeral), lower surface 16 (FIG. 1, also seen in FIG. 4 but not called out by reference numeral); specification--page 3, lines 10-16.

"a coverlay formed of a flexible organic material and laminated on the first surface of the substrate and having at least one opening formed by photolithography": Coverlay 38 (FIG. 1, FIG. 4), top surface 14 (FIG. 1), substrate 12 (FIG. 1), opening 40 (FIG. 1); specification, page 4, lines 1-9.

"at least one conductive connection formed through one of the coverlays and connecting one of the ICs to another of the ICs": metal 46 (FIG.1, FIG. 4), coverlays 38 (FIG. 1, FIG. 4), ICs 106 (FIG. 4); specification, page 9, lines 10-13; page 4, lines 9-14.

"each IC is positioned in an opening of a respective one of the coverlays": ICs 106 (FIG. 4), openings 40 (FIG. 1, also seen in FIG. 4 but not called out by reference numeral), coverlays 38 (FIG. 1, FIG. 4); specification, page 4, lines 9-10.

"all of said each IC being in said opening of said respective one of the coverlays": ICs 106 (FIG. 4), opening 40 (FIG. 1, also seen in FIG. 4 but not called out by reference numeral), coverlays 38 (FIG. 1, FIG. 4).

Claim 37

"An apparatus": Electronic apparatus 120 (FIG. 5); specification, page 9, lines 24-25.

"stacked integrated circuit (IC) package": Stacked IC package 100 (FIG. 4, FIG. 5); specification--page 9, lines 1-2.

"a first substrate": Substrate 12 (FIG. 1, FIG. 4); specification--page 9, lines 7-8.

"a first IC mounted on a first surface of the first substrate": IC 106 (FIG. 4), top surface 14 of substrate 12 (FIG. 4, FIG. 1); specification--page 9, lines 7-8.

"a first ground plane formed on an opposite surface of the first substrate from the first surface on which the first IC is mounted": Ground plane 28 (FIG. 1, also seen in FIG. 4 but

not called out by reference numeral), lower surface 16 (FIG. 1, also seen in FIG. 4 but not called out by reference numeral); specification--page 3, lines 10-16.

"a first coverlay of a flexible organic material and laminated on the first surface of the first substrate and having at least one opening formed by photolithography": Coverlay 38 (FIG. 1, FIG. 4), top surface 14 (FIG. 1), substrate 12 (FIG. 1), opening 40 (FIG. 1); specification, page 4, lines 1-9.

"a second substrate positioned in stacked fashion on the first coverlay: Substrate 12 (FIG. 1, FIG. 4), coverlay 38 (FIG. 1, FIG. 4); specification--page 9, lines 7-8.

"a second IC mounted on a first surface of the second substrate": IC 106 (FIG. 4), top surface 14 of substrate 12 (FIG. 4, FIG. 1); specification--page 9, lines 7-8.

"a second ground plane formed on an opposite surface of the second substrate from the first surface on which the second IC is mounted": Ground plane 28 (FIG. 1, also seen in FIG. 4 but not called out by reference numeral), lower surface 16 (FIG. 1, also seen in FIG. 4 but not called out by reference numeral); specification--page 3, lines 10-16.

"a second coverlay laminated on the first surface of the second substrate and having at least one opening formed by photolithography": Coverlay 38 (FIG. 1, FIG. 4), top surface 14 (FIG. 1), substrate 12 (FIG. 1), opening 40 (FIG. 1); specification, page 4, lines 1-9.

"at least one conductive connection connecting the first IC to the second IC and passing through at least one opening in the coverlay": metal 46 (FIG.1, FIG. 4), coverlays 38 (FIG. 1, FIG. 4), ICs 106 (FIG. 4); specification, page 9, lines 10-13; page 4, lines 9-14.

"a communication device coupled to at least on of the first IC and the second IC": communication device 122 (FIG. 5), ICs 106 (FIG. 4); specification, page9, lines 25-27.

"the first IC is positioned in an opening in the first coverlay": IC 106 (FIG. 4), opening 40 (FIG. 1, also seen in FIG. 4 but not called out by reference numeral), coverlay 38 (FIG. 1, FIG. 4); specification, page 4, lines 9-10.

"all of the first IC being in said opening formed by photolithography in the first coverlay": IC 106 (FIG. 4), opening 40 (FIG. 1, also seen in FIG. 4 but not called out by reference numeral), coverlay 38 (FIG. 1, FIG. 4).

"the second IC is positioned in an opening in the second coverlay": IC 106 (FIG. 4), opening 40 (FIG. 1, also seen in FIG. 4 but not called out by reference numeral), coverlay 38 (FIG. 1, FIG. 4); specification, page 4, lines 9-10.

"all of the second IC being in said opening formed by photolithography in the second coverlay": IC 106 (FIG. 4), opening 40 (FIG. 1, also seen in FIG. 4 but not called out by reference numeral), coverlay 38 (FIG. 1, FIG. 4).

* * * * * * *

Appellants will now map the limitations (substantially identical) of claims 40-43 (argued separately) to the disclosure of the application:

"a solder mask layer which covers the ground plane": Solder mask layer 34 (FIG. 1, also seen in FIG. 4 but not called out by reference numeral), ground plane 28 (FIG. 1, also seen in FIG. 4, but not called out by reference numeral); specification, page 3, lines 21-22.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

(1) Claims 15, 17, 18, 34 and 36 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Murayama et al. (U.S. Patent No. 6,548,330) in view of Sota (U.S. Patent No. 6,201,707).[1]

(2) Claims 40 and 42 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Murayama in view of Sota and further in view of Rokugawa et al. (U.S. Patent No. 6,441,314).[2]

Appellants are of the view that other rejections stated by the Examiner under § 103(a) do not present any issues beyond those discussed below in connection with the rejections listed above.

[1] The argument set forth below concerning this rejection is also applicable to the rejection of claims 19, 21, 22, 37 and 39 based on the Murayama, Sota and Blumenau (USP 6,421,711) references.

[2] The argument set forth below concerning dependent claims 40-43 is applicable to this rejection and also to the rejection of claims 41 and 43 based on a combination of the Murayama, Sota, Blumenau and Rokugawa references.

ARGUMENT

I. ***Applicable Law***

All of the issues in this appeal are related to rejections under 35 U.S.C. § 103(a). In these rejections, the Examiner found the claims at issue to be obvious in view of combinations of references.

The law governing application of 35 U.S.C. § 103(a) is set forth in general terms as follows in *In re Kotzab*, 217 F.3d 1365 (Fed.Cir. 2000):

> A claimed invention is unpatentable if the differences between it and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art [citing § 103(a)].

In comparing the claimed invention with the prior art, both the claimed subject matter as a whole and the references as a whole must be considered. *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143 (Fed.Cir. 1985).

The *Kotzab* case further sets out the following standards in regard to proposed combinations of references:

> [T]o establish obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion or teaching of the desirability of making the specific combination that was made by the applicant. [Citations omitted]
>
> The motivation, suggestion or teaching may come explicitly from statements in the prior art, the knowledge of one of ordinary skill in the art, or, in some cases the nature of the problem to be solved. [Citation omitted] In addition, the teaching, motivation, or suggestion may be implicit from the prior art as a whole, rather than expressly stated in the references. [Citation omitted] The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art. [Citation omitted][3]

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[3] 217 F.3d at 1370.

If a proposed modification of a prior art invention would render the invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900 (Fed.Cir. 1984) [cited in MPEP § 2143.01 V.].

Furthermore, a *prima facie* finding of obviousness cannot properly be made unless all the limitations of the claimed invention are taught or suggested by the prior art. *In re Royka*, 490 F. 2d 981 (CCPA 1974).

During examination before the PTO, claim terms are given their broadest reasonable interpretation, consistent with the specification (*In re Hyatt*, 211 F.3d 1367, 1372 (Fed.Cir. 2000); i.e., claim terms are given their plain meaning unless defined to the contrary in the specification (*In re Zletz*, 893 F.2d 319, 321 (Fed.Cir. 1989)). The plain meaning of a term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention. *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed.Cir. 2005).

II. The pending claims are not obvious in view of Murayama and the other references

Claim 15 is taken as exemplary of all of the pending claims, although certain dependent claims, namely claims 40-43, are also argued separately.

The primary issue in this case comes down to whether the Examiner has reasonably interpreted the claim term "ground plane". The Examiner apparently believes that it is reasonable to interpret this term broadly enough to encompass the interconnection pad 6 shown in FIG. 1 (for example) of the Murayama reference, and referred to, for example, at column 4, line 18 of the reference. It is appellants' contention that to interpret "ground plane" in this manner is unreasonable and contrary to the plain meaning of the term, as it would be understood by those who are skilled in the art. Consequently, the Murayama reference fails to disclose the claimed "ground plane". No other reference relied upon by the Examiner is considered by him to teach this claim limitation, and the Examiner has therefore failed to make out a *prima facie* case of obviousness, since, contrary to the requirement of the *Royka* case, at least one claim limitation is not taught or suggested by the prior art relied upon by the Examiner.

The present application contains no definition of "ground plane" to support any interpretation of that term broader than its plain meaning. The term is not unusual or obscure,

and would clearly be understood by those who are skilled in the art as referring to a metal layer of considerable extent, positioned to serve as ground in packaging or other support structure for an IC. The Examiner, however, to the contrary, apparently believes that the meaning of the term can be expanded to refer to any conductive layer on an IC package substrate. In taking this position, the Examiner disregards the plain meanings of both of the words "plane" and "ground". To one of ordinary skill in the art, the word "plane" would only be applied to an extensive region of conductive material, as exemplified by element 28 in FIG. 1 of the present application. Moreover, one of ordinary skill would also not apply the term to a conductive material region that is not positioned within the package structure in such a manner that it could serve as a ground.

The interconnection pad 6 shown in FIG. 1 and other drawings of the Murayama reference falls short in at least two respects from satisfying the claimed "ground plane" when that term is properly given its plain meaning. First of all, the interconnection pad 6 is of very limited extent, and certainly is much too small to be characterized as a plane. Secondly, the interconnection pad 6 is located so as to provide an interconnection between one IC and another IC in the stacked arrangement shown in FIG. 6 of the reference. As such, the interconnection pad 6 is completely unsuitable to serve as a ground, since it is not located in the right place to do so. Still further, if the interconnection pad 6 were really a ground plane, it would completely fail to perform its intended function of interconnecting the ICs 10 shown in FIG. 6.

To elaborate further, and taking a step back from the above analysis, the primary issue can be restated as, "Would a person of ordinary skill in the art identify the structure shown as item 6 in Murayama as a 'ground plane'?" Appellants respectfully submit that, to any fair-minded person, the only possible response to the foregoing question is a definite "No". The interconnection pad 6 in the reference simply is not a ground plane. With all respect to the Examiner, appellants do not believe this is a question upon which there can reasonably be disagreement.

Given that the references relied upon by the Examiner fail to teach or suggest the claimed ground plane, the Examiner has failed to produce a *prima facie* case for obviousness, and the rejection of all of the pending claims should therefore be reversed.

II. Separate argument in support of claims 40-43

Claim 40 is taken as exemplary of this group of claims, all of which are also believed patentable for reasons given above in regard to claim 15. The following discussion sets forth an additional, independent ground for patentability of claims 40-43.

Claim 40 adds to claim 15 the further limitation of a solder mask layer which covers the ground plane (the latter element being the subject of the discussion in the previous section of this Brief). In formulating the rejection of claim 40, the Examiner acknowledged that the Murayama reference fails to show a solder mask layer covering the so-called "ground plane" 6 shown in Murayama. The Examiner then proposed to supply this missing element by combining with Murayama teaching of the Rokugawa reference in regard to a solder resist layer 26 (FIG. 1 of the Rokugawa reference) on a pad 24 shown therein.[4] Based on this proposed combination, the Examiner apparently considered it obvious to modify Murayama's structure by covering the "ground planes" supposedly present in Murayama with a solder mask layer.

Of course the rejection of claim 40 suffers from the same basic flaw as the rejection of claim 15, namely that the interconnection pad 6 of Murayama cannot reasonably be considered to be a ground plane. But the rejection of claim 40 suffers from another flaw as well: The Examiner's proposed modification of Murayama's structure falls afoul of the doctrine that a modification which renders the modified structure unsuitable for its intended purpose cannot be considered to have been suggested by the prior art.[5] In the case of the Examiner's proposed modification, covering the interconnection pads 6 in Murayama would cause them to be insulated from below, and therefore unable to perform their intended function of providing a signal connection to a lower level of the stacked structure. The Examiner's proposed combination of references thus lacks support of a proper motivation to combine the references, and the purported *prima facie* case of obviousness with regard to claim 40 again fails.

It is therefore submitted that even if the rejection of claim 15 were upheld, the rejection of claim 40 should be reversed.

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[4] Without any justification, the Examiner chooses to refer to the pad 24 of Rokugawa as a "ground plane".

[5] See the *Gordon* case cited above at the top of page 5.

CONCLUSION

For the reasons stated above, the Examiner's rejections of claims are improper. Therefore, appellants respectfully request that the Examiner's rejections be reversed.

This Brief is filed within one month from the date of mailing of the Notification of Non-Compliant Appeal Brief, and as such, no extension of time is believed due. No fee is now believed to be due, in view of the payment of the Appeal Brief fee previously made in connection with the Appeal Brief filed on October 9, 2006. If any additional fees are due in conjunction with this matter, the Commissioner is hereby authorized to charge them to Deposit Account 50-1852. An Appendix of claims involved in this appeal is attached hereto.

If any issues remain, or if the Examiner or the Board has any further suggestions for expediting allowance of the present application, kindly contact the undersigned using the information provided below.

Respectfully submitted,

November 20, 2006
Date

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APPENDIX A--CLAIMS

1-14. (canceled)

15. An article of manufacture, comprising:

at least two integrated circuit (IC) packages in stacked relation to each other, each of the IC packages including:

a substrate;

an IC mounted on a first surface of the substrate;

a ground plane formed on an opposite surface of the substrate from the first surface on which the IC is mounted; and

a coverlay formed of an organic material and laminated on the first surface of the substrate and having at least one opening formed by photolithography; and

at least one conductive connection formed through one of the coverlays and connecting one of the ICs to another of the ICs;

wherein each IC is positioned in an opening of a respective one of the coverlays, the opening formed by photolithography, all of said each IC being in said opening of said respective one of the coverlays.

16. (canceled)

17. The article of manufacture of claim 15, wherein the coverlays are of a flexible material.

18. The article of manufacture of claim 17, wherein the substrates are of a flexible material.

19. An apparatus comprising:

a stacked integrated circuit (IC) package which includes:

a first substrate;

a first IC mounted on a first surface of the first substrate;

a first ground plane formed on an opposite surface of the first substrate from the first surface on which the first IC is mounted;

a first coverlay formed of an organic material and laminated on the first surface of the first substrate and having at least one opening formed by photolithography;

a second substrate positioned in stacked fashion on the first coverlay;

a second IC mounted on a first surface of the second substrate;

a second ground plane formed on an opposite surface of the second substrate from the first surface on which the second IC is mounted;

a second coverlay laminated on the first surface of the second substrate and having at least one opening formed by photolithography; and

at least one conductive connection connecting the first IC to the second IC and passing through at least one opening in the first coverlay; and

a communication device coupled to at least one of the first IC and the second IC;

wherein:

the first IC is positioned in an opening formed by photolithography in the first coverlay, all of the first IC being in said opening formed by photolithography in the first coverlay; and

the second IC is positioned in an opening formed by photolithography in the second coverlay, all of the second IC being in said opening formed by photolithography in the second coverlay.

20. (canceled)

21. The apparatus of claim 19, wherein the first and second coverlays are of a flexible material.

22. The apparatus of claim 21, wherein the first and second substrates are of a flexible material.

23-33. (canceled)

34. An article of manufacture, comprising:

at least two integrated circuit (IC) packages in stacked relation to each other, each of the IC packages including:

a substrate;

an IC mounted on a first surface of the substrate;

a ground plane formed on an opposite surface of the substrate from the first surface on which the IC is mounted; and

a coverlay of a flexible organic material laminated on the first surface of the substrate and having at least one opening formed in the coverlay; and

at least one conductive connection formed through one of the coverlays and connecting one of the ICs to another of the ICs;

wherein each IC is positioned in an opening of a respective one of the coverlays, all of said each IC being in said opening of said respective one of the coverlays.

35. (canceled)

36. The article of manufacture of claim 34, wherein the substrates are of a flexible material.

37. An apparatus comprising:

a stacked integrated circuit (IC) package which includes:

a first substrate;

a first IC mounted on a first surface of the first substrate;

a first ground plane formed on an opposite surface of the first substrate from the first surface on which the first IC is mounted;

a first coverlay of a flexible organic material laminated on the first surface of the first substrate and having at least one opening formed in the first coverlay;

a second substrate positioned in stacked fashion on the first coverlay;

a second IC mounted on a first surface of the second substrate;

a second ground plane formed on an opposite surface of the second substrate from the first surface on which the second IC is mounted;

a second coverlay of a flexible organic material laminated on the first surface of the second substrate and having at least one opening formed in the second coverlay; and

at least one conductive connection connecting the first IC to the second IC and passing through at least one opening in the first coverlay; and

a communication device coupled to at least one of the first IC and the second IC;

wherein:

the first IC is positioned in an opening in the first coverlay, all of the first IC being in said opening in the first coverlay; and

the second IC is positioned in an opening in the second coverlay, all of the second IC being in said opening in the second coverlay.

38. (canceled)

39. The apparatus of claim 37, wherein the first and second substrates are of a flexible material.

40. The article of manufacture of claim 15, further comprising:

a solder mask layer which covers the ground plane.

41. The apparatus of claim 19, further comprising:

a first solder mask layer which covers the first ground plane; and

a second solder mask layer which covers the second ground plane.

42. The article of manufacture of claim 34, further comprising:

a solder mask layer which covers the ground plane.

43. The apparatus of claim 37, further comprising:

a first solder mask layer which covers the first ground plane; and

a second solder mask layer which covers the second ground plane.

APPENDIX B - EVIDENCE

No evidence is being submitted with this Appeal Brief (*i.e.*, this appendix is empty).

APPENDIX C - RELATED PROCEEDINGS

No prior or pending appeals, interferences, or judicial proceedings are known to Applicants, Applicants' legal representative, or assignee, which may be related to, directly affect, be directly affected by, or have a bearing on the Board's decision in the pending appeal. Therefore, there are no copies of decisions rendered by a court or the Board to attach (*i.e.*, this appendix is empty).